REMARKS

The Office Action mailed September 12, 2003, has been carefully considered. In response to the Office Action, Applicants have amended the Abstract, and submit the following remarks addressing the prior art rejections.

Art Rejection Under 35 U.S.C. § 103(a)

Claims 1-3 and 11 were rejected under 35 U.S.C. § 103(a) as unpatentable over Liu et al. (U.S. Pat. No.5,425,036) in view of Pisciotta et al. (U.S. Pat. No. 4,144,448).

Claims 1 and 11 are directed to a verification system and method. In Claim 1, the system is controlled by a master clock, and includes reception logic, evalucation logic, and

> . . . clock generation logic for generating a plurality of asynchronous clocks for use by the evaluation logic and controlling the phase relationship among the plurality of asynchronous clocks.

Claim 11 contains similar language directed to the verification method.

Liu et al. is directed to a system for debugging reconfigurable emulation systems. Liu et al uses a vector comparison approach to determine whether an FPGA (field programmable gate array) configuration has been properly implemented from a source netlist, without having to recompile the netlist itself. The vector comparison consists of applying input vectors to the FPGA and thereby generating output vectors. The output vectors are compared with previously derived output vectors. If the comparison fails, "read-back" trigger instructions corresponding to fail points are inserted in the input vectors, which are then re-applied to the FPGA. These instructions facilitate capture of internal states of the FPGA, which are then analyzed in order to determine the failure sources.

The same approach can also be used when the FPGA is coupled to a target system which fails during emulation. In this case, the read-back instructions again

provide FPGA internal state information. However, this information is correlated to the target system, and the debugging can be performed with respect to the target system to find flaws therein.

Importantly, the actual emulation runs in Liu et al. are conducted in a conventional manner. This is evidenced by the paragraph entitled "Operating Step" appearing in column 7, lines 20-29, which states:

> The configured reconfigurable circuit (CRC) 250, 260 is operated by applying thereto electrical stimuli, such as digital input vector signals 12A. The stimuli may include data and clock signals which are applied to CRC 250, 260 from target system 300 or debugware 280 through interface pods 279. This stimuli application causes CRC 250, 260 to function logically and generate actual response or output signals 211.

There is no mention in Liu et al. of the use of "clock generation logic for generating a plurality of asynchronous clocks for use by the evaluation logic and controlling the phase relationship among the plurality of asynchronous clocks," as set forth in Claim 1 of Applicants' invention. To the extent that the clocking mechanism is disclosed in Liu et al., it is described as being a clock signal which is fed to the reconfigurable circuit (CRC) 250, 260 from either the target system 300 or the debugware 280. This connection is illustrated in FIG. 2, which shows a direct broken line between CLKOUT of debugware 280 and CLKIN of LBM 250, or alternatively, between the third POD 279 interfacing with target system 300 and CLKIN of LBM 250. No other clock sources are taught or suggested by Liu et al..

The failure of Liu et al. to teach or suggest the use of "clock generation logic for generating a plurality of asynchronous clocks for use by the evaluation logic and controlling the phase relationship among the plurality of asynchronous clocks" derives from Liu et al.'s disinterest in the speed of the emulation process. In other words, the system of Liu et al. is designed in accordance with the prior art devices discussed in page 4 of the written description of the present invention, and is characterized by an evaluation time which must be long enough to handle the worst possible evaluation time

needed for the inputs to be processed and stabilize at the output. As discussed in the written disclosure, for most input sequences to a conventional design such as that of Liu et a., only a very small percentage (about 1%) of the inputs require the worst possible evaluation time. Therefore, essentially 99% of all inputs are subject to the longer-than-necessary evaluation times. Further, a large percentage (about 80%) of all the inputs require less than 1/100 of the worst possible evaluation time. Similarly, a significant percentage (about 20%) of all the inputs require between 1/100 and 1/10 of the worst possible evaluation time. Thus by designing the evaluation cycle for the worst possible time, as is done in conventional designs such as that of Liu et al., the logic evaluator is forced to execute in the slowest possible speed, a speed which is not warranted by 99% of its inputs. Clearly, this is very wasteful and inefficient.

The present invention recognizes the wasteful and inefficient nature of conventional designs, and provides instead clock signaling which is dynamically generated, and customized for the particular emulation process. A detailed description of this novel design appears under the headings "DYNAMIC LOGIC EVALUATION" (page 145) and "EMULATION SYSTEM WITH MULTIPLE ASYNCHRONOUS CLOCKS" (page 151). In accordance with this design, the logic emulation system adjusts itself to the *shortest* evaluation time, generating clocks in the logic emulator to control both the logic emulator execution and the external test bench (target system). The clocks are generated using a generator clkgen 2871 (FIG. 92), relying on the clock scheduler and slices depicted in FIGS. 94-96. Importantly, the clocking signals are asynchronous, with their phase relationships being tightly controlled without regard to their actual durations, because it is recognized that only the inputs from the phase relations are of value to the emulation process. In this manner, the other components of the clock cycle—namely, their periods and durations—can be disregarded, thereby foreshortening the emulation process for most emulation runs.

The office action proposes a combination of Liu et al. with Pisciotta et al. However, it is respectfully submitted that there is no motivation for such a combination, even if such combination were to advance the obviousness basis of the

prior art rejection, a point which is not conceded, as discussed further below. One of ordinary skill in the art would not be motivated to combine Liu et al. with Pisciotta et al. because Liu et al. fails to recognize the aforementioned prior art problem arising from the need to accommodate the worst possible evaluation time. Liu et al., by not even identifying the problem with which the present invention attempts to deal, would certainly not motivate the ordinarily skilled artisan to seek its solution.

In any case, that solution is not to be found in Pisciotta et al., which is directed to a system for checking the validity of clock signals of separate conductors in systems such as microprocessors, programmed logic arrays (PLAs), or motor-driven magnetic data recording devices. Pisciotta et al. shows a testing system 12 which uses a multiplicity of flip-flops and latches (40-43, 56-7, 59-60) to lock in the states of clock signals on conductors of a system being tested. The locked-in states of the clock signals in the flip-flops and latches are used to set counters (38) which are incremented by pulses from a multipurpose oscillator 26. A frequency-divided signal P2 from multipurpose oscillator 26 provides these pulses. The counters each have a prescribed duration, and are each driven by the P2 signal. As long as the counters are not timed-out, the clock pulses are deemed valid. When a counter times out, however, the associated clock is deemed invalid and corrective action is taken.

In Pisciotta et al., there is no "clock generating logic for generating a plurality of asynchronous clocks," or for "controlling the phase relationship among the plurality of asynchronous clocks." (Claim 1) The use of the term "asynchronous" in Pisciotta et al. is merely with reference to the relationship of the signals from the multipurpose oscillator 26 of *the testing device* to the signals from the master clock oscillator 19 of *the device being tested.* As for the clock signals within the testing system 12, these all derive from the multipurpose oscillator 26, as provided via line P2, described as being at 3.5 MHz. No asynchronicity is taught or suggested in the manner set forth in Claim 1. The reason for this is because the testing system 12 is tied to the system being tested, and the testing process cannot be accelerated or compressed, by relying only on phase differences irrespective of clock periods or durations, since the system being

tested has a set clock operating speed whose acceleration, even if possible, would undermine the purpose of the test, which is to ascertain the validity of the clocks under *normal* operating conditions. Therefore even if one of ordinary skill in the art were to combine the teachings of Liu et al. with those of Pisciotta et al., the result would not anticipate nor render obvious the presently claimed invention. In any case there is no motivation for such a combination, for the reasons discussed above, and further because Pisciotta et al. is directed to a clock testing system which is not related to emulators or to any type of design automation, and therefore one of ordinary skill in the art would not look to the teachings of Pisciotta et al. in order to address problems associated with emulation systems such as that of Liu et al.

Conclusion

In view of the preceding discussion, Applicants respectfully urge that Claims 1-3 and 11 of the present application define patentable subject matter and should be passed to allowance. Such allowance is respectfully solicited.

If the Examiner believes that a telephone call would help advance prosecution of the present invention, the Examiner is kindly invited to call the undersigned attorney at the number below.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

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By: 

Kal Shami
Registration No. 38,745

P.O. Box 1404
Alexandria, Virginia 22313-1404
(650) 622-2300